

Princess Sumaya University for Technology
Computer Engineering Dept.
22541 - Computer Architecture - Fall 2023



جامعة سميرة
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Quiz 5

Duration: 5 minutes.

Name: Solution

Instructions: - No questions allowed.

-Show your work.

Question 1:

(4 Points)

Given the following information for a cache:

I-cache miss rate = 1%

D-cache miss rate = 2%

Miss penalty = 100 cycles

Base CPI (ideal cache) = 1

Load & stores are 30% of instructions

a) Calculate the Miss cycles per instruction caused by **I-cache misses/instruction**?

$$0.01 \times 100 = 1$$

b) What is the effective CPI?

$$\begin{aligned} CPI_{eff} &= 1 + 0.01 \times 100 + 0.3 \times 0.02 \times 100 \\ &= 1 + 1 + 0.6 = 2.6 \end{aligned}$$

Question 2:

(6 Points)

I. Which of the following concepts will be dominant when accessing instruction in a memory?

- ☒ a) Spatial Locality
- ☐ b) Temporal Locality

II. Which of the following RAM types has a smaller size per bit?

- ☐ a) SRAM
- ☒ b) DRAM

III. In a DDR RAM, we have separate DDR inputs and outputs.

- ☐ a) True
- ☒ b) False

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Name: Solution

Quiz 5

Duration: 5 minutes.

Instructions: - No questions allowed.

-Show your work.

Question 1:

(4 Points)

Given the following information for a cache:

I-cache miss rate = 2%

D-cache miss rate = 1%

Miss penalty = 100 cycles

Base CPI (ideal cache) = 2

Load & stores are 40% of instructions

a) Calculate the Miss cycles per instruction caused by **I-cache misses/instruction**?

$$0.02 \times 100 = 2$$

b) What is the effective CPI?

$$\begin{aligned} CPI_{eff} &= 2 + 0.02 \times 100 + 0.4 \times 0.01 \times 100 \\ &= 2 + 2 + 0.4 = 4.4 \end{aligned}$$

Question 2:

(6 Points)

I. In a DDR RAM, we have separate DDR inputs and outputs.

a) True

☒ b) False

II. Which of the following concepts will be dominant when accessing instruction in a memory?

a) Temporal Locality

☒ b) Spatial Locality

III. Which of the following RAM types has a larger size per bit?

a) DRAM

☒ b) SRAM