



Name: Solution

Quiz 4

Duration: 5 minutes.

Instructions: - No questions allowed.

-Show your work.

Question 1:

(4 Points)

What is the most appropriate value for the control signals when the following instructions are in the CPU?

Instruction	MemRead	RegWrite
Beq x1, x2, L1	0	0
ld x3, 20(X2)	1	1
And x2, x3, x4	0	1
sd x3, 20(X2)	0	0

Question 2:

(6 Points)

In a pipelined processor, if the delay (in ns) of the individual stages is given as shown below:

IF: 350 ID: 200 EXE: 150 MEM: 250 WB: 200

A. What is the clock period of this processor? 350

B. How long would a Store instruction take? $350 \times 5 = 1750$

C. If we split the Mem stage into 2 stages (each take half the time). Repeat part (b):

$$350 \times 6 = 2100$$



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Question 1:

(4 Points)

What is the most appropriate value for the control signals when the following instructions are in the CPU?

Instruction	RegWrite	MemRead
Lw x2, 20(X2)	1	1
Beq x1, x2, L1	0	0
Or x3, x1, x5	1	0
sw x3, 20(X2)	0	0

Question 2:

(6 Points)

In a pipelined processor, if the delay (in ns) of the individual stages is given as shown below:

IF: 150 ID: 300 EXE: 150 MEM: 400 WB: 200

A. What is the clock period of this processor? 400

B. How long would a branch instruction take? 5 * 400 = 2000

C. If we split the MEM stage into 2 stages (each take half the time). Repeat part (b):

6 * 300 = 1800