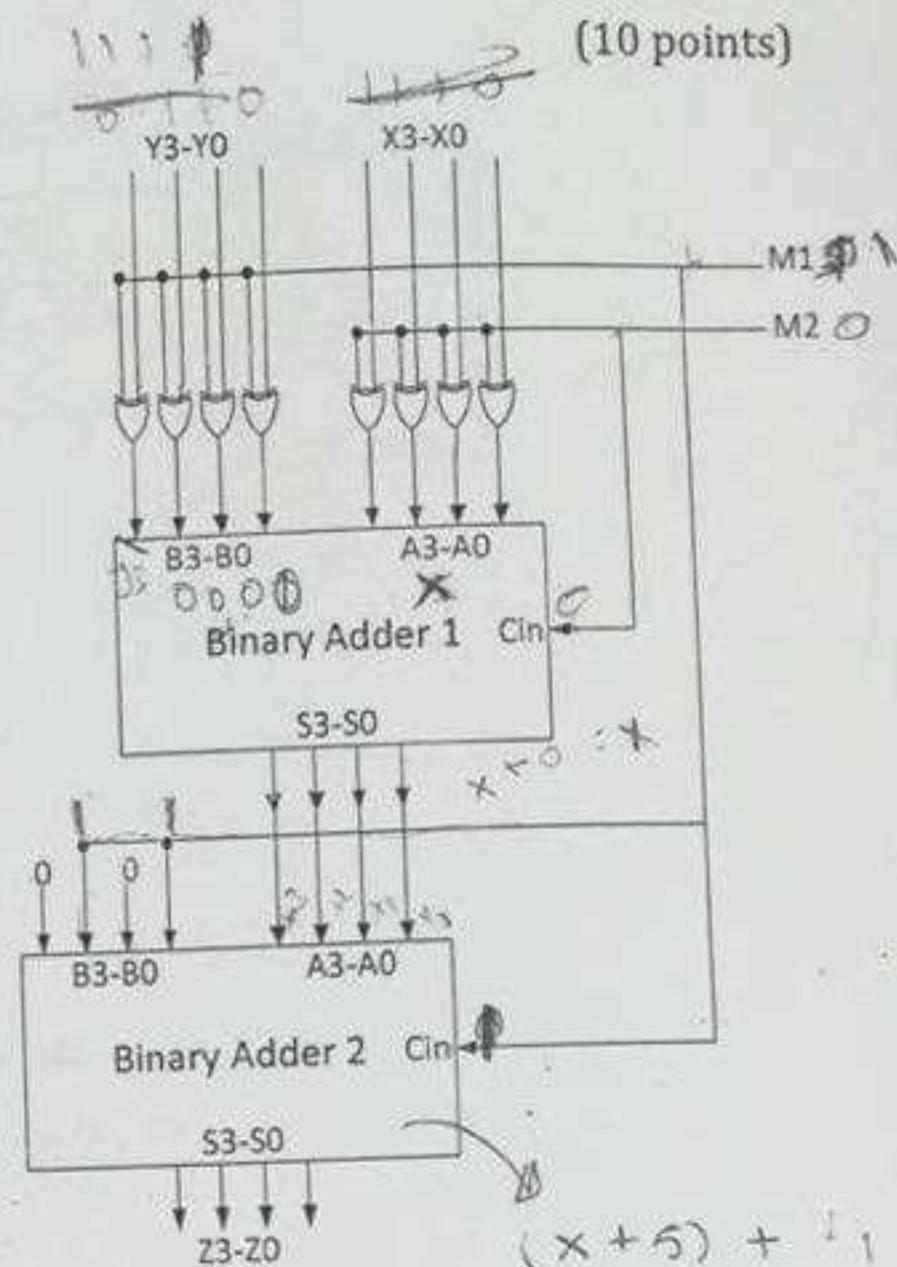


Question 4: Combinational Circuits

Use the circuit to the right, to answer Q21-Q25:



21) If ($M1=0, M2=0$) then the output of the second adder (Z) will be:

- a) $Z=Y-X$
- ☒ b) $Z=X+Y$
- c) $Z=X-Y$
- d) $Z=-X-Y$
- e) We can't tell

22) If ($M1=0, M2=1$) then the output of the second adder (Z) will be:

- ☒ a) $Z=Y-X$
- b) $Z=X+Y$
- c) $Z=X-Y$
- d) $Z=-X-Y$
- e) We can't tell

23) To make Z equal the 2's Complement of X then we need to:

- a) Set $M1=1, M2=1$ and $y=(0000)$.
- b) Set $M1=0, M2=0$ and $y=(0001)$.
- ☒ c) Set $M1=0, M2=1$ and $y=(0000)$.
- d) Set $M1=0, M2=1$ and $y=(1111)$.
- e) Can't be done via this circuit.

24) We can perform the Operation $X-Y$ if we:

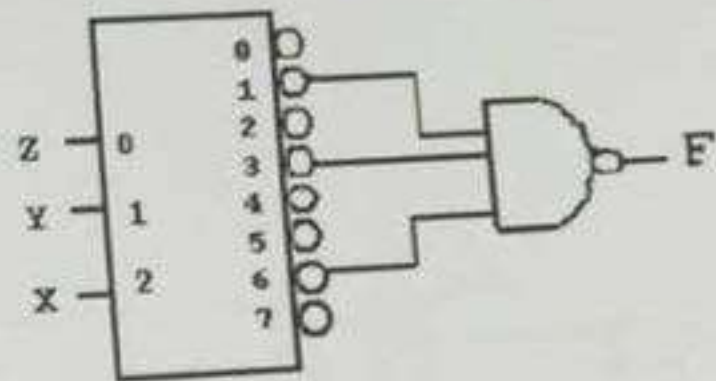
- a) Set $M1=1$ and $M2=1$.
- b) Set $M1=1$ and $M2=0$.
- c) Set $M1=0$ and $M2=1$.
- ☒ d) Can't be done via this circuit.
- e) Either a+c will work

25) The operation $X+6$ can be performed via this circuit if:

- ☒ a) Set $M1=0, M2=0$ and $y=(0110)$.
- b) Set $M1=1, M2=1$ and $y=(0110)$.
- c) Set $M1=1, M2=0$ and $y=(1111)$.
- d) Can't be done via this circuit.
- ☒ e) Either a or c

25. The function $F(x, y, z)$ implemented using the decoder shown next can be expressed as (decoder outputs are active low as shown):

- $\Sigma (1, 3, 6)$
- $\Sigma (0, 2, 4, 5, 7)$
- $\Pi (1, 3, 6)$
- $\Pi (0, 2, 4, 5, 7)$
- Non of the above



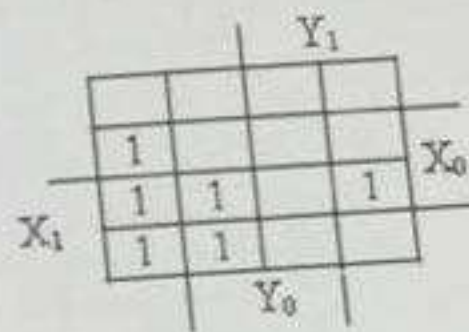
26. The minimum number of flip flops needed to build a counter that counts in the following sequence $8 \rightarrow 10 \rightarrow 12 \rightarrow 14 \rightarrow 8 \rightarrow \dots$ is:

- 2
- 3
- 4
- 5

e) non of the given answers

27. Simplifying the shown K-map to minimum number of variables would result in:

- $X_1 Y_1' + X_0 Y_1' Y_0' + X_1 X_0 Y_0'$
- $X_1 Y_1 + X_0 Y_1 Y_0 + X_1 X_0 Y_0$
- $X_1' Y_1 + X_0' Y_1 Y_0 + X_1' X_0' Y_0$
- $X_1' Y_1' + X_0' Y_1' Y_0' + X_1' X_0' Y_0$
- Non of the above



28. Its desired to design a 4-bit shift register with parallel load capability. The register is to have the following four modes of operation: parallel load, shift right, shift left, no change. What are the necessary components needed to design the register:

- four D flip-flops only
- four D flip-flops and one 4x1 multiplexer
- four D flip-flops and four 4x1 multiplexers
- one D flip-flop and four 4x1 multiplexers
- one D flip-flop and one 4x1 multiplexer

29. The size of the ROM that will accommodate the truth table for a BCD-to-Seven-segment display decoder is :

- 4 x 7 ROM
- 4 x 16 ROM
- 16 x 7 ROM
- 16 x 4 ROM
- 16 x 128 ROM

30. Referring to the characteristic table of the JK flip flop, the characteristic equation for the complement output of the JK flip-flop can be expresses as :

- $Q'(t+1) = J Q + K Q$
- $Q'(t+1) = J Q' + K Q$
- $Q'(t+1) = J' Q + K Q'$
- $Q'(t+1) = J Q + K' Q'$
- $Q'(t+1) = J' Q' + K Q$

14. A function $F(A, B, C, D, E) = BC'D$, then the expression for the function F as sum of minterms is:

- a) $F(A, B, C, D, E) = \sum(5, 13, 21, 29)$
- b) $F(A, B, C, D, E) = \sum(10, 11, 12, 13)$
- c) $F(A, B, C, D, E) = \sum(10, 11, 26, 27)$
- d) $F(A, B, C, D, E) = \sum(10, 11)$
- e) Non of the above

15. The number of flip flops that will be complemented in a 10 bit count up binary counter to reach the next count after the count 1110010111:

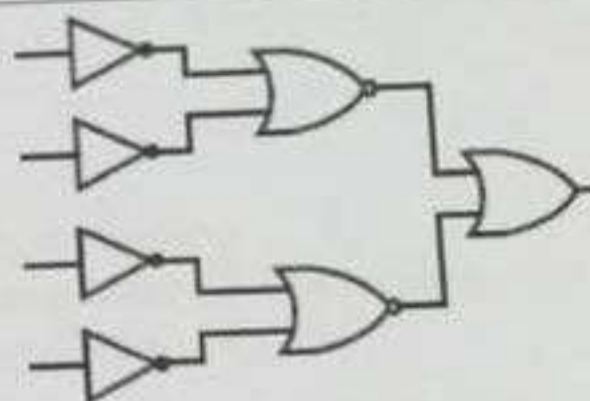
- a) 10
- b) 2
- c) 4
- d) 3
- e) 5

16. Given the numbers $(1000100)_2$, $(1000003)_8$, $(1000002)_{10}$, $(1000001)_{16}$:

- a) $(1000100)_2$ is the smallest
- b) $(1000002)_{10}$ is the biggest
- c) $(1000100)_2$, $(1000003)_8$, and $(1000001)_{16}$ have equal value
- d) Two of the given numbers are equal
- e) Non of the above is true

17. The shown circuit can be rebuilt using a minimum of:

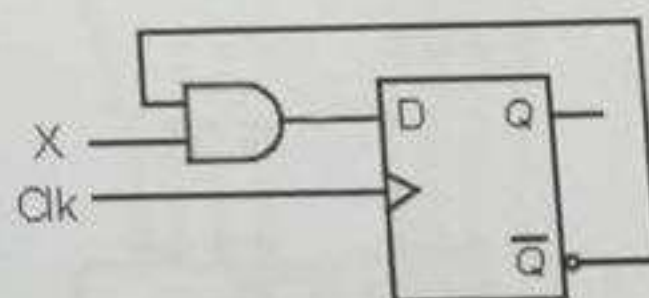
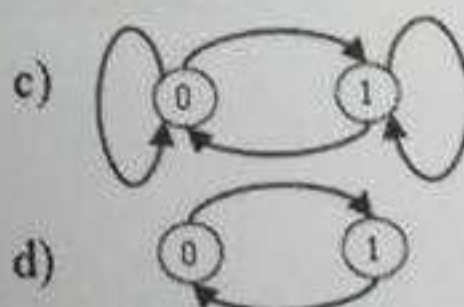
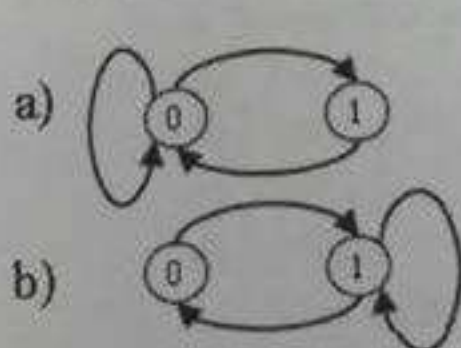
- a) 4 NAND gates
- b) 5 NAND gates
- c) 4 NAND and 1 NOR gates
- d) 3 NAND gates
- e) Non of the above



18. To implement the Boolean function $F = A \oplus B \oplus C$ we can use a 3-to-8 decoder and connect:

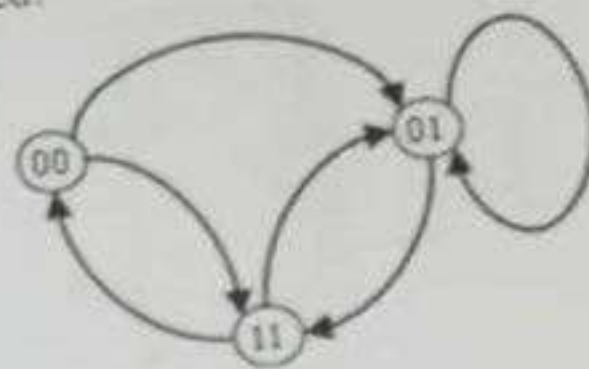
- a) 6 different lines from its output to an OR gate
- b) 5 different lines from its output to an OR gate
- c) 3 different lines from its output to an OR gate
- d) 4 different lines from its output to an OR gate
- e) 7 different lines from its output to an OR gate

19. The correct state diagram for the circuit shown is:



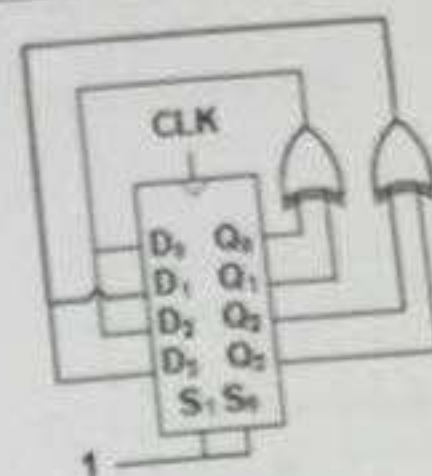
20. Two 'T' Flip-Flops, A and B, are used to implement the shown state diagram.
To go from state "AB = 01" to "AB = 11" we need:

- a) $T_A = 1, T_B = 0$
- b) $T_A = 0, T_B = 1$
- c) $T_A = 0, T_B = 0$
- d) $T_A = 1, T_B = 1$
- e) $T_A = 1, T_B = \text{don't care}$



21. A Universal Shift Register, USR, is connected as shown.
 $S_1=1, S_0=1$ select the load operation. Initially $Q_3Q_2Q_1Q_0 = 1010$. After 2 clock cycles:

- a) $Q_3Q_2Q_1Q_0 = 0000$
- b) $Q_3Q_2Q_1Q_0 = 1010$
- c) $Q_3Q_2Q_1Q_0 = 0101$
- d) $Q_3Q_2Q_1Q_0 = 1001$
- e) $Q_3Q_2Q_1Q_0 = 1111$



22. A ripple counter is a counter that:

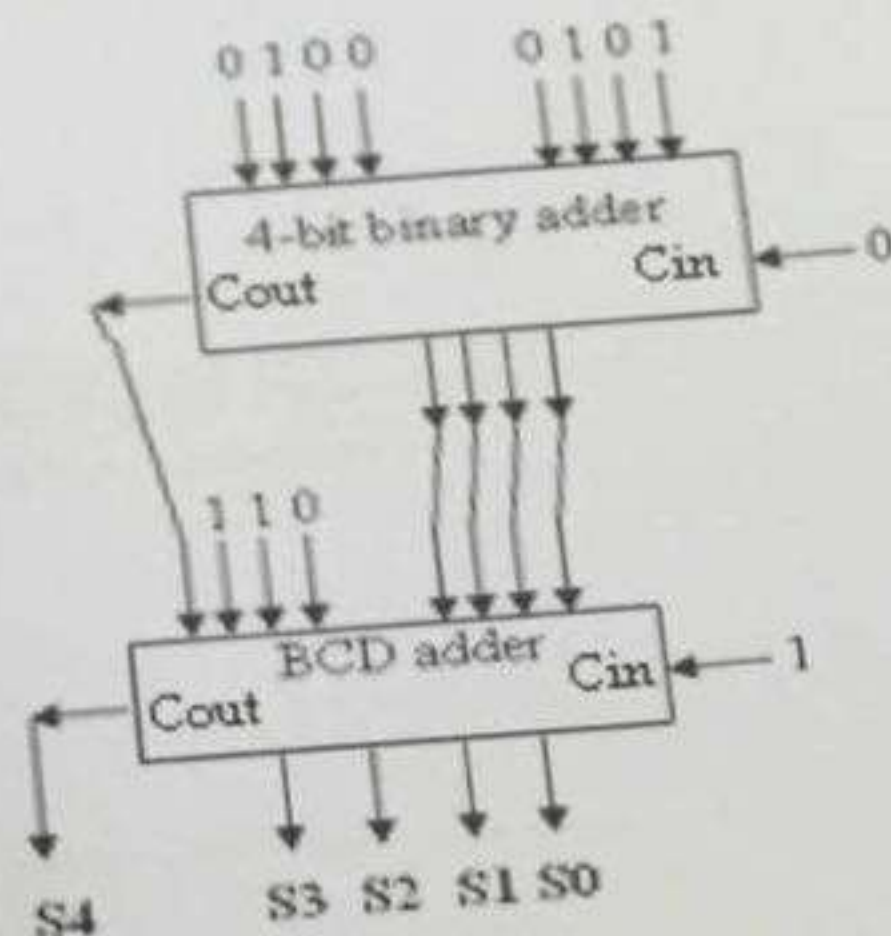
- a) works asynchronous
- b) works synchronous
- c) can be designed to work synchronously or asynchronously
- d) counts "up" synchronously and "down" asynchronously (or vice versa)
- e) counts "Binary" synchronously and "BCD" asynchronously

23. Which of these statements are true?

- a) A minterm equation is an unreduced sum-of-products Boolean expression.
- b) A minterm equation requires the least number of logic gates to implement
- c) A maxterm equation is an unreduced sum-of-products Boolean expression.
- d) A maxterm equation requires the least number of logic gates to implement
- e) Non of the above

24. The binary value of $S_4 S_3 S_2 S_1 S_0$ at the output of the circuit shown is:

- a) 10001
- b) 10000
- c) 10110
- d) 01001
- e) Non of the above



الاسم (باللغة العربية):

الشعبة: أحدى - ثلاثاء - خميس ، اثنين - أربعاء الرقم في الشعبة:

1	a	b	c	d	e
2	a	b	c	d	e
3	a	b	c	d	e
4	a	b	c	d	e
5	a	b	c	d	e
6	a	b	c	d	e
7	a	b	c	d	e
8	a	b	c	d	e
9	a	b	c	d	e
10	a	b	c	d	e
11	a	b	c	d	e
12	a	b	c	d	e
13	a	b	c	d	e
14	a	b	c	d	e
15	a	b	c	d	e
16	a	b	c	d	e
17	a	b	c	d	e
18	a	b	c	d	e
19	a	b	c	d	e
20	a	b	c	d	e
21	a	b	c	d	e
22	a	b	c	d	e
23	a	b	c	d	e
24	a	b	c	d	e
25	a	b	c	d	e
26	a	b	c	d	e
27	a	b	c	d	e
28	a	b	c	d	e
29	a	b	c	d	e
30	a	b	c	d	e
31	a	b	c	d	e
32	a	b	c	d	e
33	a	b	c	d	e
34	a	b	c	d	e
35	a	b	c	d	e
36	a	b	c	d	e
37	a	b	c	d	e
38	a	b	c	d	e
39	a	b	c	d	e
40	a	b	c	d	e

1. How many address lines and data lines are needed in a 256 K x 64 RAM:

- 18 address lines and 64 data lines
- 64 address lines and 18 data lines
- 2^{18} address lines and 64 data lines
- 256 address lines and 18 data
- Non of the above

2. Simplifying the Boolean expression $A' B (D' + C' D) + B (A + A' C D)$ would result in:

- A
- B
- D
- A+B
- Non of the given answers

3. How many BCD counters are needed to build a counter for the range 0-999:

- 1 BCD counter
- 3 BCD counters
- 9 BCD counters
- 999 BCD counters
- Non of the above

4. The decimal number 20 is expressed in Binary Coded Decimal (BCD) as:

- 1010
- 00100000
- 10101
- 10100
- Non of the above

5. The unsigned number $(AF.16C)_{16}$ is equivalent to:

- Non of the answers below is right
- $(257.0554)_8$
- $(157.0558)_8$
- $(157.0568)_8$
- $(157.0534)_8$

Question 2: Boolean Algebra

(5 points)

- 8) If X was a Boolean variable, which of the following is correct:
~~a) $X+1=X$~~ ☒ c) $X+X'=1$
~~b) $X \cdot 0=X'$~~ ☒ d) All of the above
- 9) Using Demorgan Theorem the following expression $((X'Y')+XYZ)'$ can be written as:
 a) $(XY)(X'+Y'+Z')$ c) $(X'Y')'+(XYZ)'$
☒ b) $(X+Y)(X'+Y'+Z')$ d) $(XY)+X+Y+Z$
- 10) In a Boolean function $f(x,y,z)$, minterm 5 and maxterm 6 are as follow:
 a) $m_5=x'y'z'$, $M_6=x'+y'+z$ ☒ c) $m_5=xy'z$, $M_6=x'+y'+z$
 b) $m_5=x'+y+z'$, $M_6=xyz'$ d) $m_5=x'y'z'$, $M_6=x+y+z'$
- 11) If $F(x,y,z)=\Sigma(1, 2, 3, 4)$, then the following is true:
 a) $F'=\Pi(0, 5, 6, 7)$ c) $F'=\Sigma(5, 6, 7)$
 b) $F'=\Sigma(1, 2, 3, 4)$ ☒ d) $F=\Pi(0, 5, 6, 7)$
- 12) Using Boolean manipulation, the Expression $(x+z)(x'+xy'+z)$ can be simplified to:
 a) $xz+yz$ c) $x+z$
☒ b) $xy'+z$ d) $xy'+zx$

Question 3: Gate Level Minimization

(8 points)

- 13) The sum of minterms of the function to the right is:

- a) $F = \Sigma(0,1,2,7)$
 b) $F = \Pi(0,1,2,7)$
 c) $F = \Pi(2,3,5,6)$
☒ d) $F = \Sigma(0,1,4,7)$

x	y	z	F
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

- 14) The following is a correct representation of F:

- a) $F = xy'z + xy'z'(xyz)'$
 b) $F = x'y'z' + xy'z'$
 c) $F = (x+y+z')(x+y'+z)(x+y'+z')(x'+y+z')(x'+y'+z)(x'+y'+z')$
☒ d) b and c
 e) a and c

x	y	z	F
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

$$\begin{aligned}
 & 0 + xy' + xz + x'z + y'z + z \\
 & xy' + z(x+x') + y'z + z \\
 & xy' + y'z + z \\
 & xy' + z(y'+1) \\
 & xy' + z \checkmark
 \end{aligned}$$

(7 points)

- an overflow:
- $$\begin{array}{r} 0101 \\ 0110 \\ \hline 1011 \end{array}$$

Question 5: Synchronous Circuits

(10 points)

31) Which of the following is true:

- a) Latches are edge triggered, while flip flops are level triggered.
- b) Latches and Flip Flops can be both edge or level triggered.
- c) Only D Latches are level triggered while other latched are edge triggered.
- d) Flip flops are edge triggered only if the clock is positive edge.
- ☒ e) None of the above.

32) A J-K flip-flop can be configured to work as T flip flop if we:

- a) Set $J=0$ and $K=1$.
- b) Set $J=1$ and $K=0$.
- c) Set $J=1$ and $K=1$.
- d) Can't be done!
- ☒ e) Connect J and K together

33) The characteristic equation for the J-K flip-flop is

- a) $Q(t+1) = J'Q + K'Q'$
- b) $Q(t+1) = J'Q' + K'Q$
- ☒ c) $Q(t+1) = JQ' + K'Q$
- d) $Q(t+1) = JQ + K'Q'$
- e) None of the above.

34) Which of the following is true:

- a) In Moore state machine the Output is dependent on the input only.
- b) In Moore state machine the Output is dependent on the present state only.
- c) In Mealy state machine the Output is dependent on the input.
- d) In Mealy state machine the Output is dependent on the present state.
- ☒ e) b, c and d are all correct.

35) In a J-K Flip Flop, if $Q(t) = 1$ and $Q(t+1) = 0$, then the JK values are:

- a) $J=1, K=1$
- b) $J=0, K=1$
- c) $J=0, K=0$
- d) b+c
- ☒ e) a+b

11
01

mealy
moore
present state
input
moore
present state

6. How many 256K x 8 RAMs are needed to build a 1 M x 8 RAM:

- a) 2 b) 4 c) 8 d) 16 e) 32

7. The size of an Encoder with n output lines is:

- a) $2^n \times 1$ b) $2^n \times n$ c) $n^2 \times 1$ d) $n \times 2^n$ e) Non of the given answers

8. The content of a 4-bit register is initially 1101. The register is shifted six times to the right with the serial input being 101101. What is the contents of the register after the sixth shift :

- a) 1110 b) 1011 c) 1101 d) 0111 e) Non of the given answers

9. Which of the following statements is true?

- a) Outputs of sequential circuits do not depend on previous events.
b) Outputs of combinational circuits do not depend on previous events.
c) Sequential logic devices don't contain state storage information.
d) Sequential logic devices' outputs are dependent on current inputs only.
e) Non of the given statements is true

10. Which of these devices are sequential?

- a. Exclusive-Or gate
b. Counter
c. Decoder
d. Multiplexer
e. Tri-State Buffer

11. How many binary bits are necessary to represent 748 different numbers?

- a) 7 b) 8 c) 9 d) 10 e) Non of the given answers

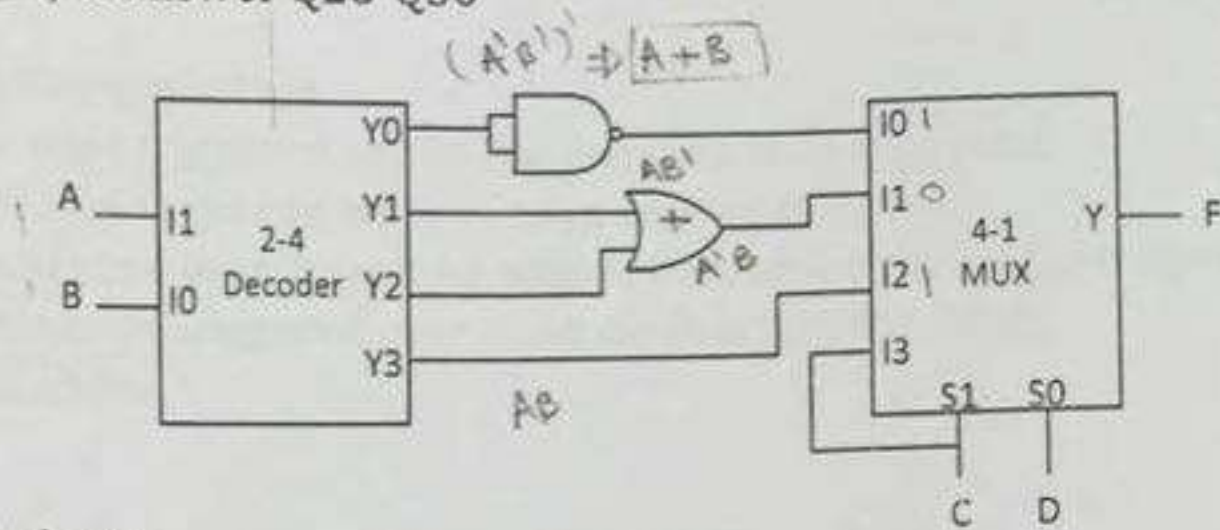
12. A logic function $F(A,B,C,D)$ was simplified without considering the don't care conditions and the expression for F was: $F = B' C' + AC'D + A' B' C + A' B D$. However, when the don't care conditions were considered the same function F is reduced to: $F = A' + C'$. The don't care minterms that are used in the simplifications are:

- a) $d(A,B,C,D) = \sum (10, 11, 14, 15)$
b) $d(A,B,C,D) = \sum (1, 6, 7, 14, 15)$
c) $d(A,B,C,D) = \sum (4, 6, 12)$
d) $d(A,B,C,D) = \sum (0, 2, 3, 4, 5, 9, 12, 13)$
e) Non of the above

13. The 7's complement for $(6235)_7$ is:

- a) $(0431)_7$ b) $(1542)_7$ c) $(1543)_7$ d) $(0432)_7$ e) Non of the given answers

Use the circuit below, to answer Q26-Q30



26) If $C=1$ and $D=1$, then :

- a) $F(A, B) = A'$
- ☒ b) $F(A, B) = 1$
- c) $F(A, B) = A + B$
- d) $F(A, B) = A \cdot B$
- e) None of the Above.

27) If $C=0$ and $D=1$, then the function $F(A, B)$ will be:

- ☒ a) $F(A, B) = A \oplus B$
- b) $F(A, B) = A + B$
- c) $F(A, B) = A \cdot B$
- d) $F(A, B) = AB + A'B'$
- e) None of the Above.

$$AB' + A'B$$

28) To make $F(A, B) = A \cdot B$, then we should:

- a) Set $C=0$ and $D=0$
- b) Set $C=0$ and $D=1$
- ☒ c) Set $C=1$ and $D=0$
- d) $a+b$
- e) Can't be done using this circuit.

$$C=1$$

$$D=0$$

29) To make $F(A, B) = A + B$, then we should:

- a) Set $C=0$ and $D=1$
- b) Set $C=1$ and $D=0$
- ☒ c) Set $C=0$ and $D=0$
- d) $a+b$
- e) Can't be done using this circuit.

$$C=0$$

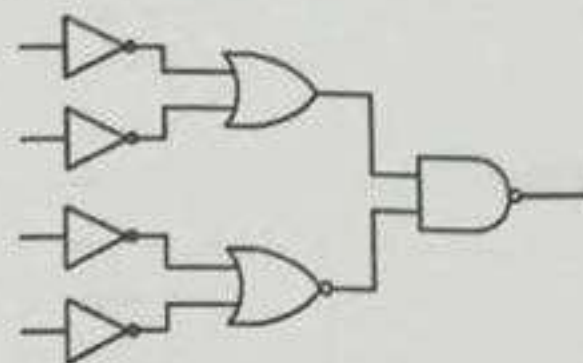
$$D=0$$

30) If we set $A=1$ and $B=1$, Then $F(C, D)$ will be =

- a) $\Sigma(1, 2)$
- b) $\Sigma(0, 2, 3)$
- c) $\Sigma(0, 1, 2, 3)$
- d) We can't tell.
- e) None of the above.

15) The following logic circuit can be implemented using a minimum of:

- a) 3 NAND gates
- b) 2 NAND gates and 1 AND gate ✓
- c) 1 AND gate 1 NAND gate and 1 OR gate
- d) a and b
- e) b and c



16) Applying the k-map method of simplification, the minimum number of circles (Prime Implicants) needed to simplify the function $F(A,B,C,D)$ in the following k-map is:

- a) 3 circles of 4 squares
- b) 3 circles of 4 squares, and 1 circle of 2 squares
- c) 2 circles of 4 squares, and 1 circle of 2 squares
- d) 1 circle of 4 squares, 1 circle of 6 squares, and 1 circle of 2 squares

3

1	1	X	0
0	1	1	0
1	X	1	X
0	X	0	0

2

17) The following k-map representation of $F(x,y,z,w)$ as a sum of minterms is:

- a) $F = \sum(0,1,2,5,12,15)$
- b) $F = \sum(0,1,5,7,12,15)$
- c) $F = \sum(0,1,6,7,12,15)$
- d) $F = \sum(0,1,5,7,12,14)$

$\sum(0,1,5,7,12,15)$

	zw				
xy		1	1	0	0
	0	1	1	0	0
	1	0	1	0	0
	0	0	0	0	0

18) The table to the right is the truth table of a:

- a) XNOR gate
- b) AND Gate
- c) XOR gate
- d) a and b

x	y	z
0	0	0
0	1	1
1	0	1
1	1	0

19) One of the following is NOT TRUE:

- a) $x \odot x = 1$
- b) $x \oplus x' = 1$ ✓
- c) $x \oplus 0 = x$ ✓
- d) $x \odot 1 = x$

20) In an even parity system, the following is used to generate the parity bit:

- a) XOR
- b) AND
- c) OR
- d) XNOR

Use the Table to the right to answer Q36-Q40

36) Which of the following is true:

- a) This is a Moore state machine.
- ☒ b) This is a Mealy state machine.
- c) Neither Mealy nor Moore.
- d) We can't tell.
- e) This is a special case, it is both machines.

37) If present state (AB=10) and the input $x = 1$, then:

- a) Next State = 10 and output = 1
- b) Next State = 01 and output = 0
- ☒ c) Next State = 11 and output = 0
- d) Next State = 11 and output = 1
- e) Next State = 01 and output = 1

38) If we are to implement this machine using T-flip flops then how many T flip-flops you need.

- a) 1
- ☒ b) 2
- c) 3
- d) 4
- e) 8

39) If we implement this Machine using D Flip Flops then $D_A(A, B, x)$ will be:

- ☒ a) $\Sigma(1, 4, 5, 7)$
- b) $\Sigma(0, 2, 3, 6)$
- c) $\Sigma(4, 5, 6, 7)$
- d) $\Sigma(0, 3, 6, 7)$
- e) None of the above

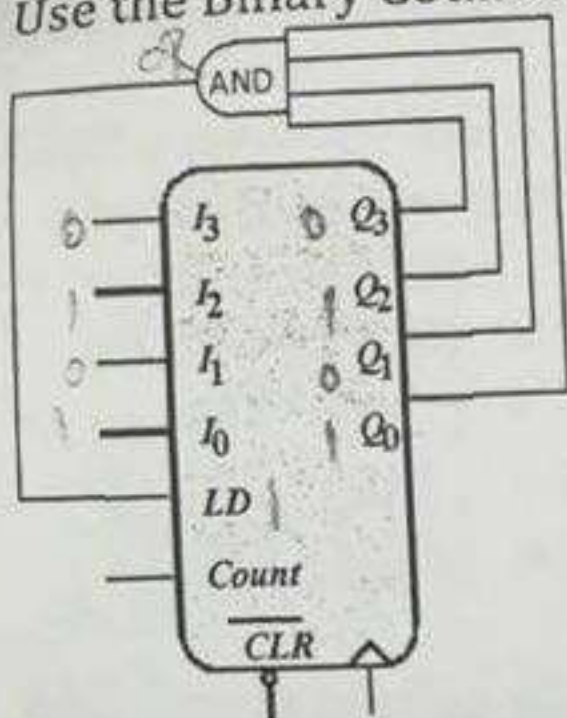
40) If we implement this Machine using T Flip Flops then $T_B(A, B, x)$ will be:

- a) $\Sigma(1, 2, 5, 6, 7)$
- ☒ b) $\Sigma(1, 3, 5)$
- c) $\Sigma(4, 5, 6, 7)$
- d) $\Sigma(0, 1, 2, 3, 6)$
- e) None of the above

Present State		Input	Next State		Output	D_A	T_B
A	B	x	A	B	y		
0	0	0	0	0	1		
0	0	1	1	1	0		
0	1	0	0	1	0		
0	1	1	0	0	1		
1	0	0	1	0	0		
1	0	1	1	1	0		
1	1	0	0	1	1		
1	1	1	1	1	1		

As Next State

Use the Binary Counter with Parallel Load answer Q44-Q46



CLR	LD	Count	$Q(t+1)$
0	x	x	0
1	0	0	$Q(t)$
1	0	1	$Q(t)+1$
1	1	x	I

44) If $I_3-I_0 = 0101$, and the counter has been running for some time, then the counter sequence will be:

- $5 \rightarrow 6 \rightarrow 7 \rightarrow 8 \rightarrow 9 \rightarrow 10 \rightarrow 11 \rightarrow 12 \rightarrow 13 \rightarrow 14 \rightarrow 15 \rightarrow 5 \rightarrow 6 \dots$
- $0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 6 \rightarrow 7 \rightarrow 8 \rightarrow 9 \rightarrow 10 \rightarrow 11 \rightarrow 12 \rightarrow 13 \rightarrow 14 \rightarrow 15 \rightarrow 0 \rightarrow 1 \dots$
- $0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 5 \rightarrow 0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 5 \dots$
- $0 \rightarrow 1 \rightarrow 0 \rightarrow 1 \rightarrow 0 \rightarrow 1 \rightarrow 0 \rightarrow 1 \rightarrow 0 \rightarrow 1 \rightarrow \dots$
- a or c depending on count.

45) Using the configuration above, If we want the counter to count from 0 \rightarrow 15, then:

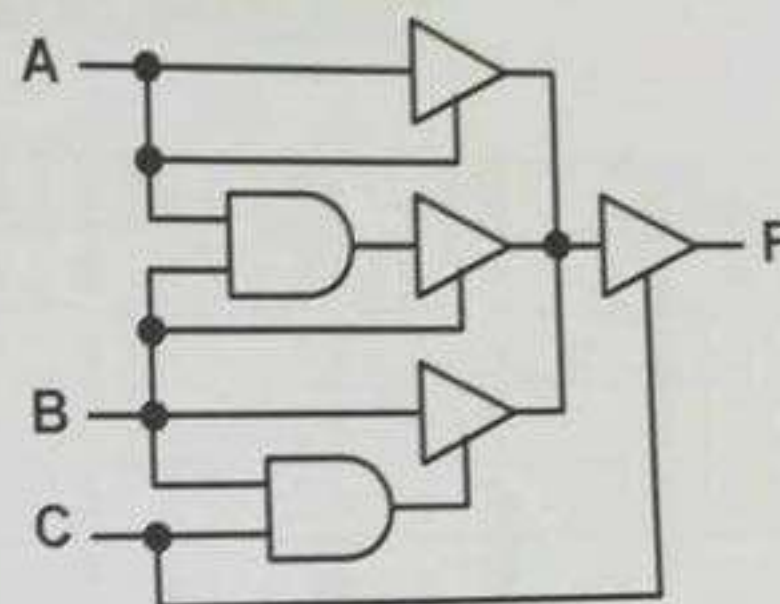
- Set $I_3-I_0 = 0000$.
- Connect the AND gates output to the CLR.
- Remove the AND gate completely.
- a+c.
- None of the above.

46) In the circuit above if the AND is replaced with an OR gate and $I_3-I_0 = 0101$, then the counter output will be:

- Does not change from AND Output.
- $1 \rightarrow 1 \rightarrow 1 \rightarrow 1 \rightarrow 1 \rightarrow 1 \rightarrow 1 \rightarrow 1 \rightarrow 1 \rightarrow 1 \rightarrow \dots$
- $5 \rightarrow 5 \rightarrow 5 \rightarrow 5 \rightarrow 5 \rightarrow 5 \rightarrow 5 \rightarrow 5 \rightarrow 5 \rightarrow 5 \rightarrow \dots$
- $0 \rightarrow 1 \rightarrow 0 \rightarrow 1 \rightarrow 0 \rightarrow 1 \rightarrow 0 \rightarrow 1 \rightarrow 0 \rightarrow 1 \rightarrow \dots$
- None of the above.

37. Referring to the figure which uses tri-state buffers, which of the following cases makes $F = 1$,

- a) $A = 0, B = 1, C = 0$
- b) $A = 0, B = 0, C = 1$
- c) $A = 1, B = 0, C = 0$
- d) $A = 0, B = 0, C = 0$
- e) $A = 1, B = 0, C = 1$



38. A 4×16 decoder can be constructed using only:

- a) Two 3×8 line decoders with "Enable" and one AND gate.
- b) Two 3×8 line decoders with "Enable" and one OR gate.
- c) Four 2×4 line decoders with "Enable".
- d) Four 2×4 line decoders with "Enable" and one Not gate
- e) Five 2×4 decoders with "Enable"

39. To add 3 operands $X + Y + Z$, each one is 4 bits wide, we need a minimum of:

- a) 8 half adders
- b) 12 half adders
- c) 4 full adders and 4 half adders
- d) 8 full adders
- e) 8 full adders and 1 half adder.

$$\begin{array}{r} X_3 X_2 X_1 X_0 \\ + Y_3 Y_2 Y_1 Y_0 \\ + Z_3 Z_2 Z_1 Z_0 \\ \hline \end{array}$$

40. Which of the following inputs are used with ROMs:

- a) input and output data lines
- b) read/write
- c) clock input
- d) all of the above are used
- e) non of the above are used

Question 7: Memory and Programmable Logic

(4 points)

47) If a memory block has 5 address lines (A_4-A_0), each memory address has a size of 2 bytes then the total number of bits in this memory is:

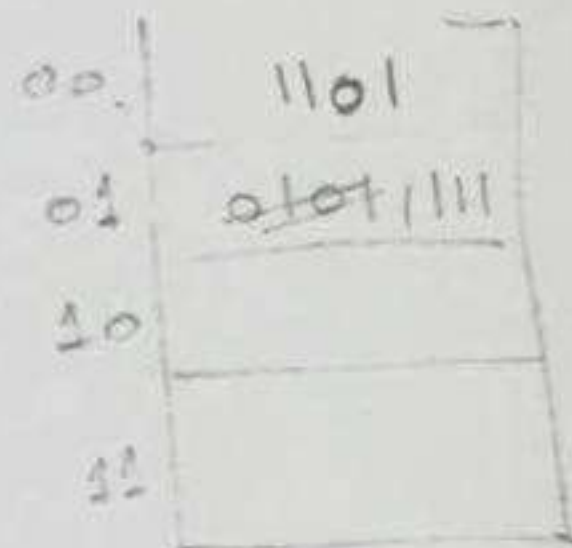
- a) $5 + (2 \times 8) = 21$
- b) $2^{5-1} * (2 \times 8) = 16 \times 16 = 256$.
- c) $2^{5-1} * (2 \times 1) = 16 \times 2 = 32$.
- d) $2^5 * (1 \times 2) = 32 \times 2 = 64$.
- e) $2^5 * (2 \times 8) = 32 \times 16 = 512$.

48) If the following sequence of events was executed on a 4x4 memory block.

- #1: Rd/Wr=0 (Write), Addr(I_1I_0)= 01, Data= 0101
- #2: Rd/Wr=0 (Write), Addr(I_1I_0)= 00, Data= 1101
- #3: Rd/Wr=1 (Read), Addr(I_1I_0)= 00
- #4: Rd/Wr=0 (Write), Addr(I_1I_0)= 01, Data= 1111
- #5: Rd/Wr=1 (Read), Addr(I_1I_0)= 00

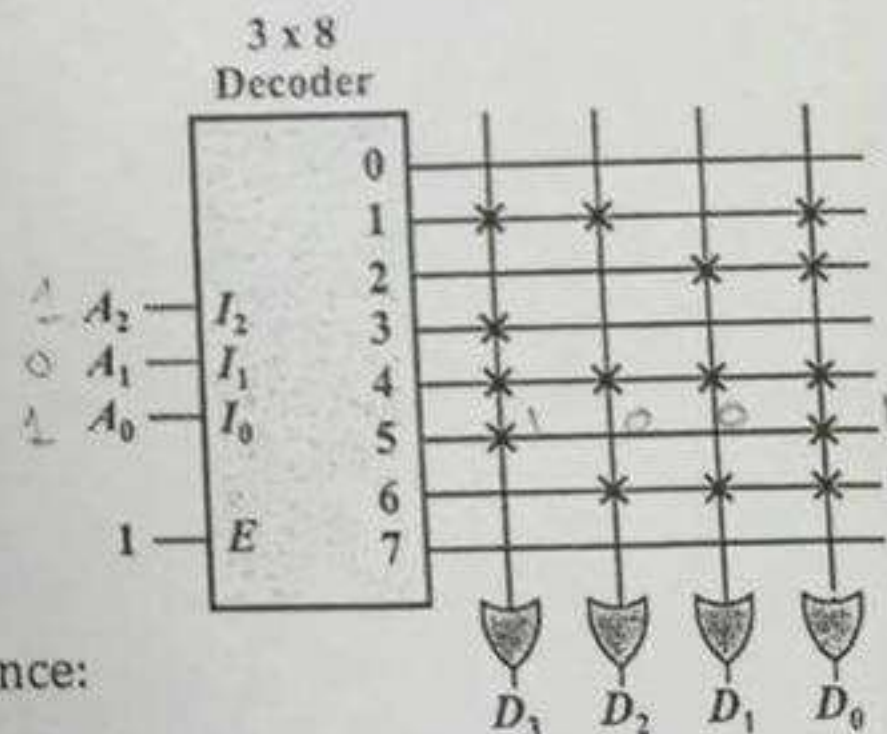
What is the value that was read in #5

- a) 0101
- b) 1111
- c) 0000
- d) 1101
- e) Unknown.



49) In the ROM shown, what value will be read if you set (A_2, A_1, A_0) = 101.

- a) 1111
- b) 0000
- c) 1001
- d) 0110
- e) None of the above.



50) Which of the following can be programmed only once:

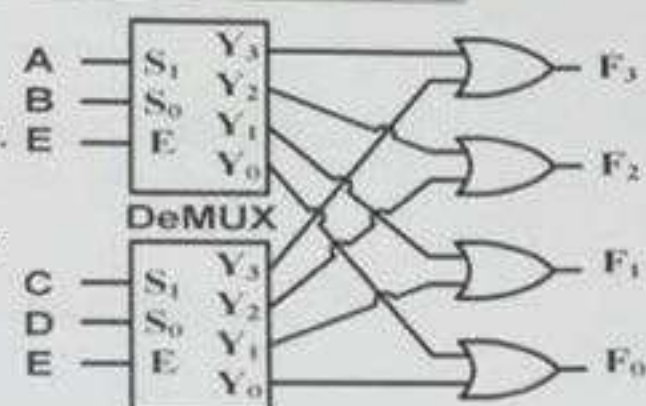
- a) Mask Programmed ROM.
- b) Programmable Read-Only Memory (PROM).
- c) Erasable Programmable ROM (EPROM).
- d) Electrically Erasable PROM (EEPROM).
- e) a and b

31. A ROM implements the following four Boolean functions: $A(x,y,z) = \sum(2,5,6)$, $B(x,y,z) = \sum(0,3,4)$, $C(x,y,z) = \sum(4,6,7)$, and $D(x,y,z) = \sum(0,1,2)$. Considering the ROM as a memory, specify the memory contents at address '5': $(101)_b$.

- a) 0000
- b) 1000
- c) 1111
- d) 0101
- e) Non of the above

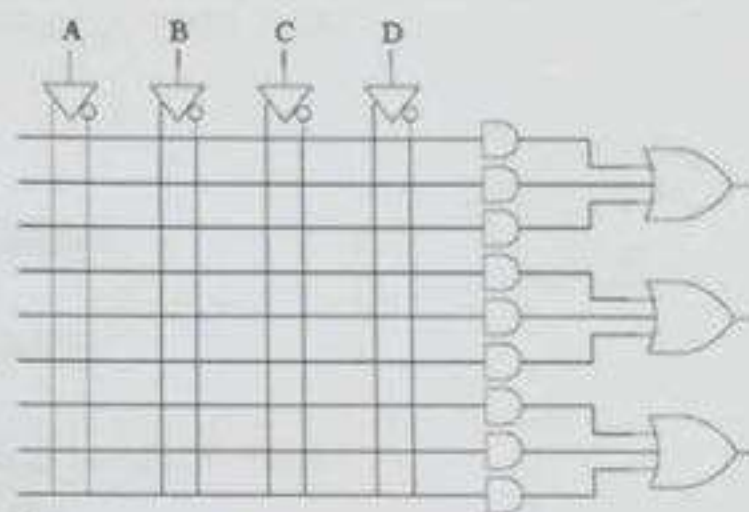
32. Consider the four outputs $F_3 F_2 F_1 F_0$, (where E is the input to the two DeMultiplexers)

- a) It is impossible to have any output = 1 at any time.
- b) Only one output can be 1 at any time.
- c) Only three outputs maximum can be 1 at any time
- d) Only two outputs maximum can be 1 at any time.
- e) All four outputs can be 1 at any time.



33. The diagram shown next represents

- a) PROM
- b) FPGA
- c) PLA
- d) PAL
- e) Non of the above



34. The value $(-53)_{10}$ represented using 8 bits in 2's complement system would be equivalent to:

- a) $(2EB)_{16}$
- b) $(FB)_{16}$
- c) $(2B)_{16}$
- d) $(CB)_{16}$
- e) Non of the above

35. Regarding bits, there are

- a) 16 in a byte
- b) 2 in a nibble
- c) 4 in a byte
- d) 4 in a nibble
- e) None of the above

36. Which one of the following statements is wrong:

- a) $x \oplus 0 = x$
- b) $x \oplus 1 = x$
- c) $x \oplus x = 0$
- d) $x \oplus x' = 1$
- e) $x' \oplus x' = 0$

Key for form (a) of Logic final for the Fall of 2010-2011

1	a	b	c	d	e
2	a	b	c	d	e
3	a	b	c	d	e
4	a	b	c	d	e
5	a	b	c	d	e
6	a	b	c	d	e
7	a	b	c	d	e
8	a	b	c	d	e
9	a	b	c	d	e
10	a	b	c	d	e

11	a	b	c	d	e
12	a	b	c	d	e
13	a	b	c	d	e
14	a	b	c	d	e
15	a	b	c	d	e
16	a	b	c	d	e
17	a	b	c	d	e
18	a	b	c	d	e
19	a	b	c	d	e
20	a	b	c	d	e

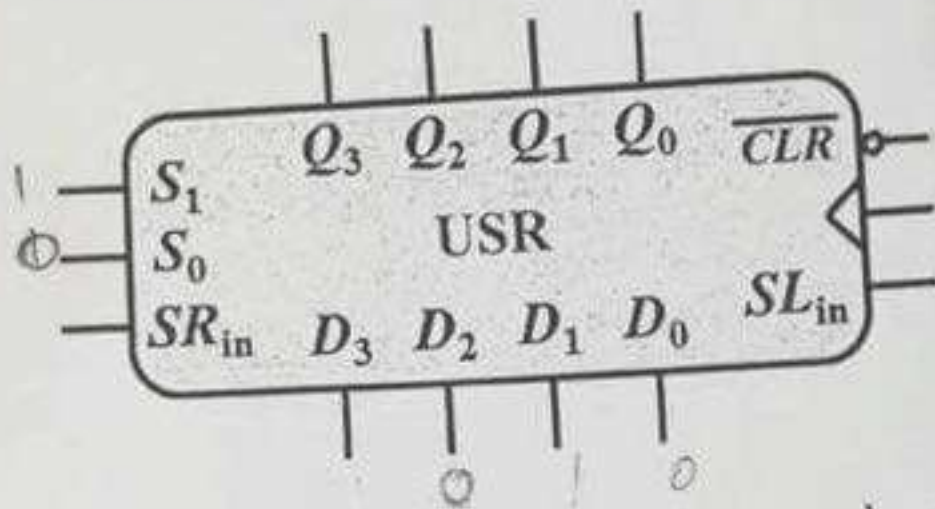
21	a	b	c	d	e
22	a	b	c	d	e
23	a	b	c	d	e
24	a	b	c	d	e
25	a	b	c	d	e
26	a	b	c	d	e
27	a	b	c	d	e
28	a	b	c	d	e
29	a	b	c	d	e
30	a	b	c	d	e

31	a	b	c	d	e
32	a	b	c	d	e
33	a	b	c	d	e
34	a	b	c	d	e
35	a	b	c	d	e
36	a	b	c	d	e
37	a	b	c	d	e
38	a	b	c	d	e
39	a	b	c	d	e
40	a	b	c	d	e

(6 points)

Question 6: Registers & Counters

Use the Universal Shift Register below to answer Q41-Q43



Mode Control		Register Operation
S_1	S_0	
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

41) To clear the register content we should:

- a) Set both $SR_{in} = 1$, $SL_{in} = 1$.
- b) Set $S_1 = 0$, $S_0 = 0$.
- ☒ c) Set CLR' to Zero. \rightarrow Inverter will
- d) Either one of a, b, c will work.
- e) None of the above.

42) What is the value in the USR (Q) after the following sequence is executed:

1st Clock: $S_1 = 1$, $S_0 = 1$, $D_3-D_0 = 1010$, $SL_{in} = 1$, $SR_{in} = 1$

- a) $Q_3-Q_0 = 1011$
- b) $Q_3-Q_0 = 1110$
- c) $Q_3-Q_0 = 0101$
- ☒ d) $Q_3-Q_0 = 1010$
- e) $Q_3-Q_0 = \text{Unknown}$

43) What is the value in the USR (Q) after the following sequence is executed:

1st Clock: $S_1 = 1$, $S_0 = 1$, $D_3-D_0 = 0110$, $SL_{in} = 1$, $SR_{in} = 1$

2nd Clock: $S_1 = 1$, $S_0 = 0$, $D_3-D_0 = 1010$, $SL_{in} = 1$, $SR_{in} = 1$

- a) $Q_3-Q_0 = 1010$
- b) $Q_3-Q_0 = 0101$
- ☒ c) $Q_3-Q_0 = 1101$
- d) $Q_3-Q_0 = 0100$
- e) $Q_3-Q_0 = \text{Unknown}$

0110
1101